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HIGH PERFORMANCE, LOW COST, SELF-CONTAINED, MULTIPURPOSE PC BASED GROUND SYSTEMS

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ABSTRACT: The use of embedded processors greatly enhances the capabilities of personal computers when used for telemetry processing and command control center functions. Parallel architectures based on the use of transputers are shown to be very versatile and reusable, and the synergism between the pc and the embedded processor with transputers results in single unit, low cost workstations of $20 < \text{MIPS} \leq 1000$.

Key Words: workstation, telemetry processing, embedded processor, transputer, parallel processing

1. INTRODUCTION

During the mid 1980's, the flight operations team for the Nimbus 7 satellite developed a ground system concept based on the following goals: low cost, highly enhanced performance, small size, short development cycles, ease of maintenance and use, reusability of software and hardware, and maximal use of commercially available parts and software. The original system used for control of the Nimbus 7 spacecraft was implemented on an IBM 8088 XT with a DOS operating system which housed an embedded processor based on the Motorola 68000 series chip. Since its implementation in 1987, these systems have evolved into Intel based 80486 type PC's with embedded processors which use transputers and modular architectures and operate under SCO UNIX in a multitasking mode. These systems are all data base driven. An individual unit can acquire data at rates in excess of 2 megabits, frame synch it, and perform health and safety analysis, perform all command functions, post pass analysis of all playback data, Level 0 processing, data distribution and archive functions. Section 2 discusses transputers (Ref. 1) and our use of embedded processors in detail and sections 3 and 4 discuss our total integrated ground station.

To date, these systems have been or will be developed and implemented for:

a) The operation of the Nimbus 7 satellite since OCT 1987, at a cost saving of more than \$750,000 per year with less than one day of accumulated down time. Development and testing were completed in less than 2 years.

b) An instrument control center in less than 15 months for the Total Ozone Mapping Spectrometer (TOMS) flown on a Russian Meteor-3 spacecraft on August 15, 1991. To date, more than 99.99% of transmitted data has been captured and distributed.

c) An interface between the NASA communications network and up to ten principal investigators' ground systems in less than 12 months in support of the Global Geospace Satellites' Wind & Polar missions in mid 1991. This was our first on line transputer system.

d) A complete flight operations control center for support of the TOMS Earthprobe mission scheduled for launch in mid 1994.

e) A programmable Telemetry, Command & Archive system for Nimbus 7 operations in less than 8 months. It replaced an equivalent system which occupied 1000 sq. ft. in May 1992.

The transputer is a parallel architecture (Ref. 1) computing device with its own direct communications channels. This allows modular design of the telemetry interface board which results in several tasks to occurring simultaneously such as data ingest and archive, command and verify, and health and safety checks. In practice, we use two or more systems in a cluster mode to perform total spacecraft operations with full redundancy, and due to both hardware and software being identical, systems can be interchanged and perform any required function. In our applications, they are connected via an internal

LAN to a mission planning terminal and a server for data distribution to the Science operations facility. Today's transputers have up to 30 Million Instructions Per Second (MIPS) peak (Ref.1) power and are used for number crunching activities and high speed bit operations, while the Intel based host 80486 computer provides a programming communications interface to the transputer and controls graphic displays and data bases. It is expected that 200 MIPS transputers (Ref 2.) will be available in the near future and this system design will make use of this increased power without the need for redesign.

2. EMBEDDED PROCESSORS

A transputer is the basic building block for a PC based system architecture. The transputer provides both computational power and communication channels which makes it possible to transfer data in a nonbus mode. Transputers feature a built-in hardware scheduler which enables any number of concurrent processes to share the processors time and have well defined growth paths to future technologies. This makes a very powerful and versatile component for Parallel Processing.

Scalable communications band-width is an equally important feature for a parallel architecture. A transputer has four direct DMA link engines which provide highly efficient mechanisms for inter-processor communications and data transfers while avoiding the limitations of a shared memory design. The transputer's DMA links and the ease of integration provides the methodology to support design of functional modular building blocks. In PC based workstations, modularity is the key factor in developing a scalable , cost effective and reliable system as shown in figure 1. Custom modules such as the NASCOM interface, Computation modules, SCSI modules, and Ethernet modules are a few of the modular building blocks utilized in PC based ground stations.

Embedded computers which use Transputers feature a parallel architecture, which in turn provides the ability to expand (or scale) the hardware configuration to suit the application. Parallel Processing relies on the effective utilization of multiple processors for increased performance.

In a PC based ground system, a favorable ratio of computation to communication between processors indicates a good fit for parallel implementations. Problems such as real-time control, monitoring, event

determination, image, and science processing have proven to be good candidates for Parallel Processing.

3. SYSTEM ARCHITECTURE

The current system architectural concepts are:

a.) The host computer's primary function is to provide the programming interface to the embedded system and provide a graphical user interface. The user interface either utilizes a DOS/Windows or UNIX/X-Windows/Motif environment depending on the applications requirements.

b.) The embedded processor provides the systems computational power. Employing 30 MIPS peak (Ref. 1) processing rate per transputer, and capitalizing on the busless point to point communications channels, a network of local task solvers can operate simultaneously. The embedded processor becomes a building block permitting a flexible approach to providing data capture, health and safety analysis, commanding, and science processing all on the same system. As higher speed transputers come on the market, they can replace or compliment slower speed modules.

c.) The use of Commercial Off The Shelf (COTS) hardware and software is maximized and that Industry Standards are utilized for all external interfaces.

A typical system in today's environment consists of an Intel based 80486 host computer with the SCO UNIX Open Desktop operating system and support equipment as diagramed in Figure 2. A special purpose, full length, 32 bit Extended Industry Standard Architecture (EISA) board featuring Bus Mastering Protocol has been designed to provide support of parallel processing. The EISA board provides module sites to support up to ten parallel processing modules as diagramed in Figure 1. The EISA board with the appropriate modules, serves as a front end NASCOM interface with capabilities of hi-speed data capture and archive to disk or tape, frame synchronization and building, cyclic redundancy checks, and packetized data transfer. Other functions such as telemetry processing, calibration, event/mode determination and mode dependent limit checking may be implemented. This provides expandable parallel processing sized to the application. Up to four boards may be installed inside an Intel based 80486 host. Connections are

provided to interface with external based Massively Parallel Processing (MPP) systems (scalable up to 800 Giga-Instructions Per Second (GIPS)) when greater computational capacity is required (Ref. 3). Industry Standard interfaces are utilized and include;

- a) Small Computer Systems Interface (SCSI)
- b) RS-422 and RS-232
- c) Ethernet IEEE 802.3 File Transfer Protocol (FTP), and Transmission Control Protocol (TCP/IP)

4. SYSTEM APPLICATIONS

The system architecture diagramed in figure 2 provides a building block approach to ground system requirements whether it be a stand alone or distributed application. Typically in the stand alone system, one system is used for commanding and another for health and safety analysis. A hot redundant back up for each of the two prime systems prevents a single point of failure and low cost protection for data or commanding loss. Command management, scheduling, and spacecraft software image maintenance is performed on another system with redundant back up. All systems are networked together via ethernet for data distribution, data archive, and strip chart recording. This self contained, integrated system, provides spacecraft command and control capabilities on a desktop and uses standard office power and environmental services.

The use of commercially available software and hardware for data-bases and displays reduces documentation efforts and helps control cost. For example, Case tools are used in the development cycle, word processors are used to develop displays, and FoxPro is used to generated the databases for database driven software. Use of these standard tools reduces learning time both for operators and designers.

The small size does not mean reduced performance. During the pass, real time commanding and command verification based on telemetry returns occur while receiving and processing satellite data. All spacecraft systems are continuously checked and monitored. Icons using color to designate status change are continuously displayed and are selectable for full on

screen viewing by a keystroke. Other features which add to this system performance are;

- a) The capability to do X-Y plots on any telemetry point for trend analysis.
- b) Highlighting status changes due to command or events on any display.
- c) Sub-system sorted chronological by event or mode list.
- d) Use of optical disks for long term data archiving.
- e) Level '0' science processing can be performed post pass or real time depending on the missions needs.

To convert a standalone system to a distributed system, both an ethernet module and compute module are added to the Embedded Controller board. Packets of information are distributed to numerous display terminals using a client-server mode similar to the X-Windows environment. This is well suited for multi-spacecraft operations or applications where multi instrument displays are necessary to support scientist and experimenters.

In summary, the use of personal computers in combination with high speed transputer modules provides a relatively low cost, highly versatile, workstation building block upon which satellite control centers can be built.

5. REFERENCES

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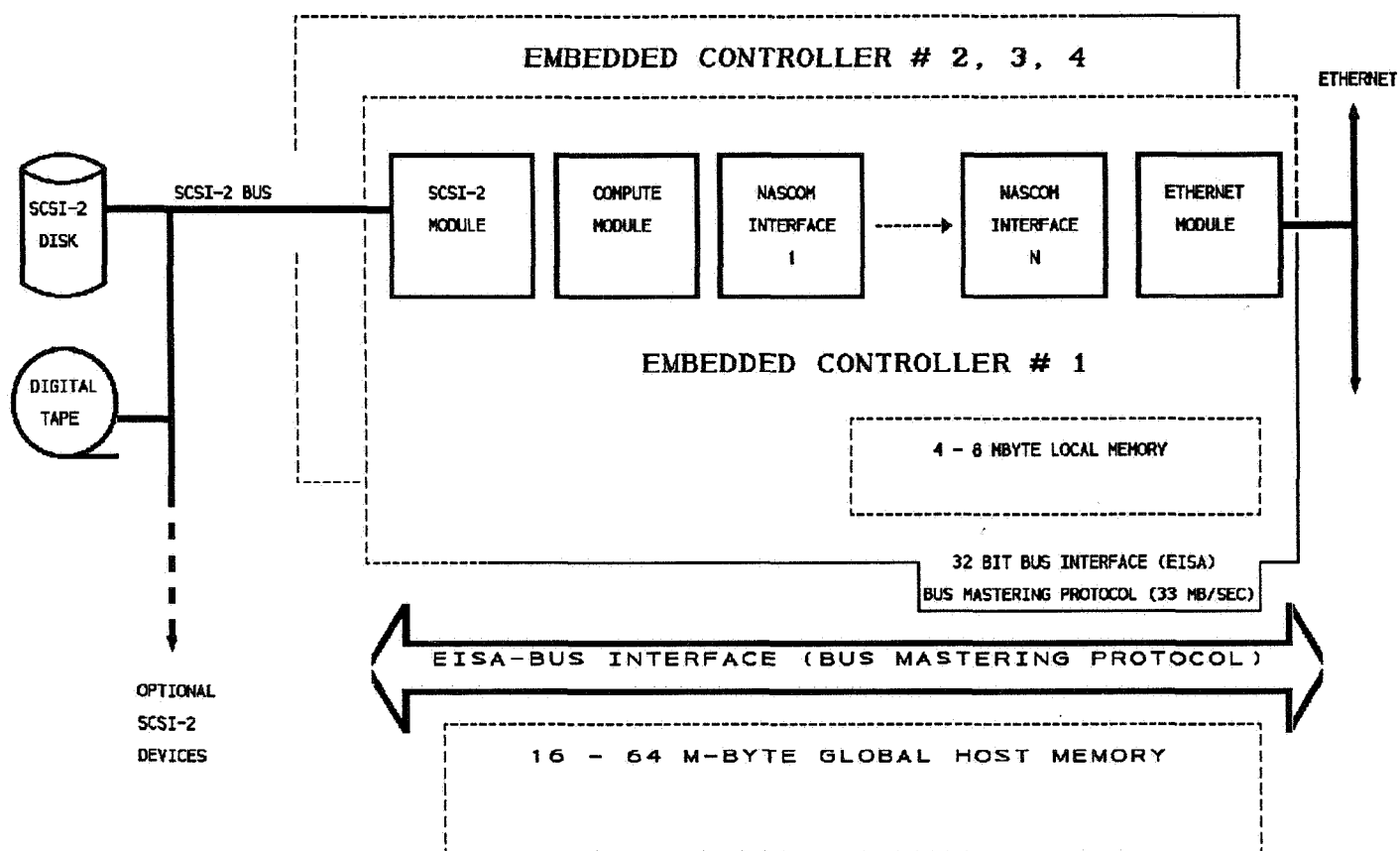
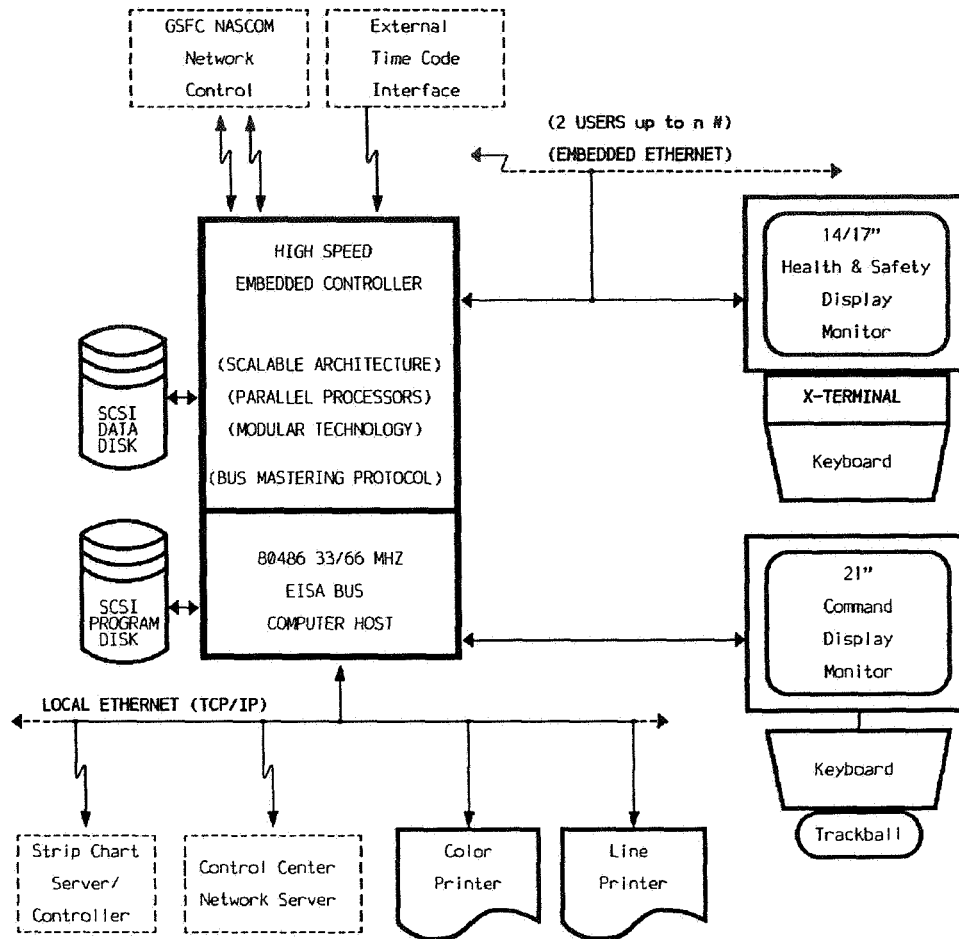


Figure 1. Embedded EISA-BUS Architecture



SCSI - SMALL COMPUTER SYSTEMS INTERFACE EISA - EXTENDED INDUSTRY STANDARD ARCHITECTURE

EMBEDDED CONTROLLER FUNCTIONS

- Expandable Parallel Processing
- Data Ingest: Up to 5.0 Mbit/sec
- Network Deblocking & Data Synchronizing
- High Speed Data Archive Support
- Telemetry Decommutation
- Quality Check of Data
- CRC Encoding / Decoding
- Asynchronous Data Synchronization
- Time Tagging
- Clock Error Determination
- Data Transmit: Up to 1.544 Mbit/sec

HOST FUNCTIONS

- Unix Based Multi-User / Multi-Tasking System
- X-Window Graphical User Interface (GUI)
- Color Video Capture & Print Support
- Strip Chart Recorder Support
- Data Sampling With X-Y Plots
- Trend Analysis
- Telemetry Processing and Display
- Alarm Determination
- Event Determination
- Event Smoothing
- Limit Checking
- Mode Determination
- Gray Code Conversions
- Command Creation, Edit, Validation
- Command Verify
- System Control
- Data Base Management

Figure 2. System Design Concept